

D3.14 - AML accelerator prototype implementations – Initial

This work demonstrates the initial prototype implementation of a high-performance hardware accelerator for Algebraic Machine Learning (AML) and usage guidelines. designed Hardware design uses a template architecture from Deliverable D3.13. Xilinx Vivado HLS tool has been utilised to design the hardware architecture. Xilinx Vivado tool synthesis and generate binary file to program FPGA. FPGAs, specifically Xilinx Alveo U280, provide the ideal platform for experimentation due to their flexibility and high memory bandwidth. The hardware setup includes FPGA bitstream generation and software compilation with specific drivers. The software offloads computation to the FPGA, with data transferred to FPGA HBM memory via PCIe. CPU instructions initiate FPGA tasks, with results available post-execution. Data transfer to server memory may be needed for result retrieval. In conclusion, this work aims to implement a hardware accelerator for AML and provides a user interface that can be used to call within AML training or inference in order to address the huge performance requirement of AML.